

*AMENDMENTS TO THE SPECIFICATION*

Replace the paragraph beginning at page 1, line 24 with:

Here, when this connection cable 3 between the inverter 1 and the motor 2 is long, a surge voltage exceeding twice a direct-current bus voltage Vdc may occur at cable-connection ends of the motor 2. That is, the connection cable 3 can be considered as a resonant circuit composed of a wiring inductance and a floating capacitance. When the connection cable 3 is long, the wiring inductance and the floating inductance are both increased, thereby reducing a resonant frequency of the resonant circuit. As a result, before resonance excited at the resonant circuit due to a stepwise change in voltage produced by the inverter 1 is attenuated, the next stepwise change in voltage is applied. Such repeated application increases resonance, thereby causing a surge voltage, which is a voltage higher than usual, at the ~~cable~~ cable connection ends of the motor ~~1~~ 2.

Replace the paragraph beginning at page 20, line 10 with:

Selection of the type of combination of the voltage vectors V0 to V7 is performed as shown in Fig. 8 according to the phase  $\theta$  in the current PWM control cycle T. As shown in Fig. 8, the phase  $\theta$  has six ranges, that is,  $0 \leq \theta < \pi/3$ ,  $\pi/3 \leq \theta < 2\pi/3$ ,  $2\pi/3 \leq \theta < \pi$ ,  $\pi \leq \theta < 4\pi/3$ ,  $4\pi/3 \leq \theta < 5\pi/3$ , and  $5\pi/3 \leq \theta < 2\pi$ . The number of voltage vectors to be selected is four out of eight, but the combination of them varies for each range of the phase  $\theta$ . However, the zero-voltage vectors ~~to~~ V0 and ~~to~~ V7 are always included in any combination.

Replace the paragraph beginning at page 51, line 15 with:

The eighth embodiment describes an exemplary measure (steps ST81 to ~~ST84~~ ST85) ~~to~~ for details (inconveniences) taken as an exception and not considered in the

power-converter control apparatus shown in the first embodiment (Fig. 4) when the output times of the zero-voltage vectors are adjusted to zero as described in the second embodiment (Fig. 15).

Replace the paragraph beginning at page 55, line 4 with:

In Fig. 26, at step ~~90~~ ST90 in place of the first step ST51 shown in Fig. 20, the voltage vectors V1, V2, V0, and V7 input from the voltage-vector control unit 11, the output times t1, t2, t0, and t7, the voltage vectors V1\_p, V2\_p, V0\_p, and V7\_p, which are adjusted outputs input from the delay unit 32 at one previous PWM control cycle, and their output times t1\_p, t2\_p, t0\_p, and t7\_p are read. Then, when the output times of the zero-voltage vectors are adjusted to zero at step ST57 or ST 58, it is determined whether the voltage vector last output at the previous time is identical to the voltage vector to be first output at this time (step ST91).

Replace the paragraph beginning at page 55, line 14 with:

As a result, when the voltage vector last output at the previous time is identical to the voltage vector to be first output at the present time (step ST91: Yes), this is the case of (3)' described above, and therefore no process is performed and then the procedure goes to step ST93. On the other hand, when the voltage vector last output at the previous time is different from the voltage vector to be first output at this time (step ST91: No), this is the case of (4)'. Therefore, the voltage vector to be first output at the present time is changed to the vector last output at the previous time (step ST92), and the procedure goes to step ST93. At step ST93, the adjusted output times t1', t2', t0', and t7' of the voltage vectors and the voltage vectors V1', V2', V0', and V7' are output. When the procedure goes to step ~~93~~ ST93 from any one of steps ST12, ST54, and ST 55, the voltage vectors V0, V1, V2, and V7 selected by the voltage vector controlling unit 11 are directly output as the voltage vectors V0', V1', V2', and V7' to the firing-pulse generating unit 13.